CORE
- Functional
  - Microprocessor
    - PowerPC
    - Other microprocessor family
  - DMA Controller
  - Filter
- Structural
  - Bus Arbiter
    - Max Number of Masters
    - Max Number of Slaves
  - Master Device
    - Bus Type
  - Slave Device
    - Bus Type
- Electrical
  - Operator Frequency
  - Implementation Type
    - Hard Core
    - Soft Core
    - Firm Core
- Other characteristics

PIN
- Functional
  - Data Type
    - Address
    - Instruction
  - Function Type
    - Read
    - Write
  - Operation Type
    - Request
    - Acknowledge
- Structural
  - Bus Type
    - Processor Local Bus
    - Peripheral Bus
  - Interface Type
    - Master
    - Slave
  - Resource Type
    - Bus
    - Peripheral
- Electrical
  - Operating Frequency
  - Drive Characteristics
    - Input
    - Output
    - Bidi
  - Capacitive Load
- Other characteristics

FIG. 1

PIN ———

———— INTERFACE_DEF ————

—— Bus Type

—— Interface Type

—— Function Type

—— Operation Type

—— Data Type

—— Resource Type

—— Pin Group Type

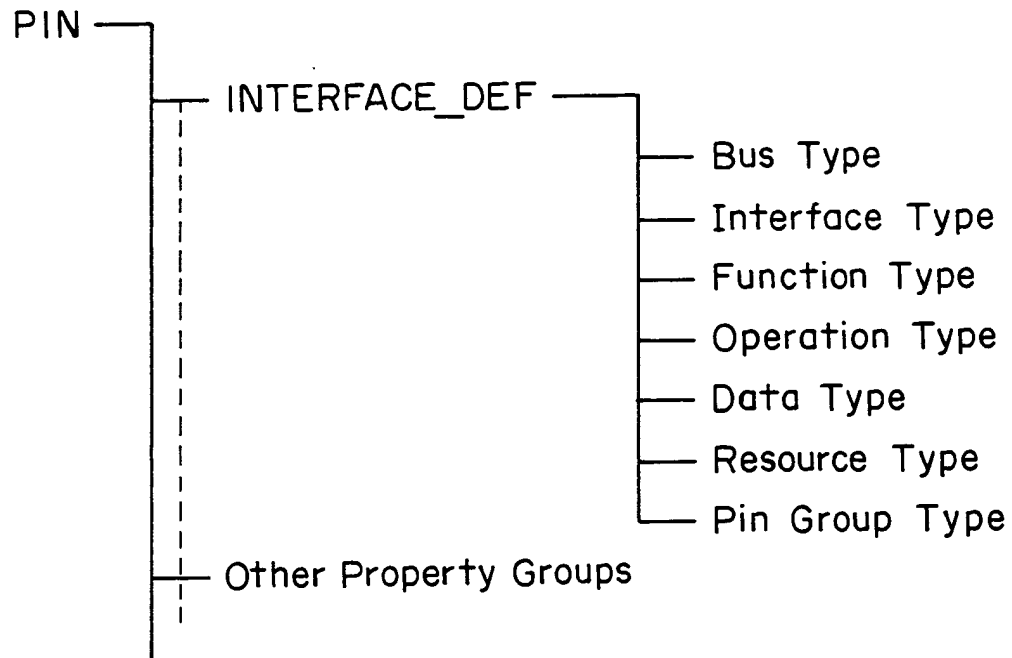—— Other Property Groups

FIG. 2

```
COMPONENT PowerPC401 PROPERTIES{

   COMPOSITE_PROPERTY INTERFACE_DEF{
      PROPERTY BUS_TYPE: {PLB, OCM, DCR, ect.};

      PROPERTY INTERFACE_TYPE: {MASTER, ISOCM, DSOCM, SYSTEM, EIC., I.SSD, JTAG,...};

      PROPERTY FUNCTION_TYPE: {READ_OR_WRITE, READ, WRITE, INTERRUPT, FETCH,...};

      PROPERTY OPERATION_TYPE : { ACKNOWLEDGE, BUSY, ERROR, VALID, ABORT, ENABLE,
                            GUARDED_TRANSFER, COMPRESSED_TRANSFER, REQUEST,
                            SIZE, BYTE_ENABLE, ADJUST, HOLD,...}

      PROPERTY DATA_TYPE: { ADDRESS, DATA, PRIORITY_DATA, INSTRUCTION,...};

      PROPERTY RESOURCE_TYPE: {BUS, WRITE_BUS, READ_BUS,...};

      PROPERTY PIN_GROUP/L: {DCU, ICU, IN, OUT, CONROL,...};
   };

   PROPERTY CONNECTION_LOGIC: {CONCAT, OR, AND, XOR, NOT };

   pin ICU_plhRequest {
         INTERFACE_DEF= {PLB, MASTER, FETCH, REQUEST, INSTRUCTION, BUS, ICU };
   };
   pin PLB_dcuAddrAck{
         INTERFACE_DEF= {PLB, MASTER, READ_OR_WRITE, ACKNOWLEDGE, ADDRESS,
                      BUS, DCU};
   };
   pin PLB_icuRdDBus{
         INTERFACE_DEF= {PLB, MASTER, READ, NA, DATA, BUS, ICU};
   };
   pin DCR_cpuAck{
         INTERFACE_DEF= {DCR, NA, READ_OR_WRITE, ACKNOWLEDGE, DATA, NA, CONTROL};
         CONNECTION_LOGIC= { OR };
   };
   ......
   ......
```
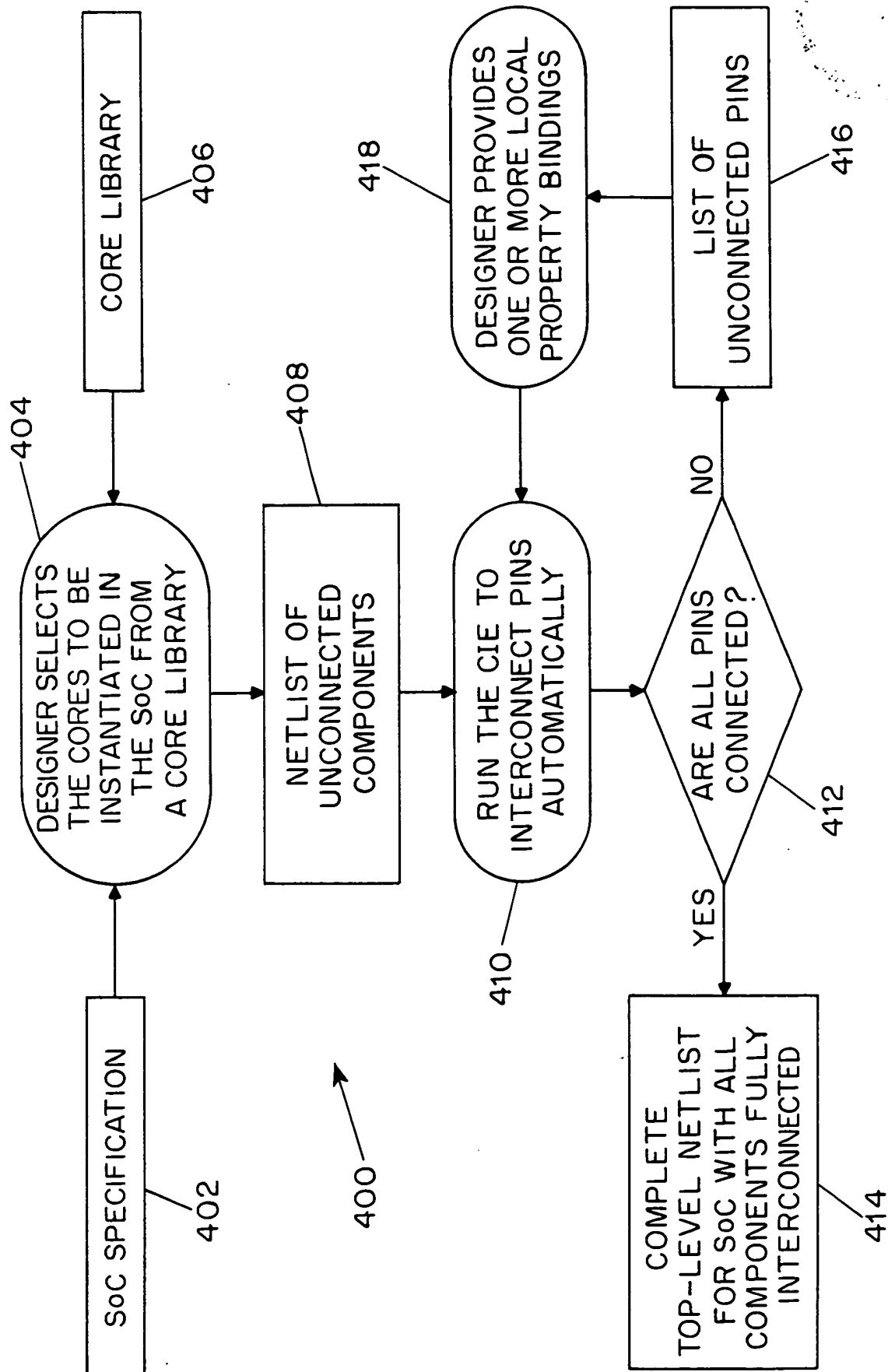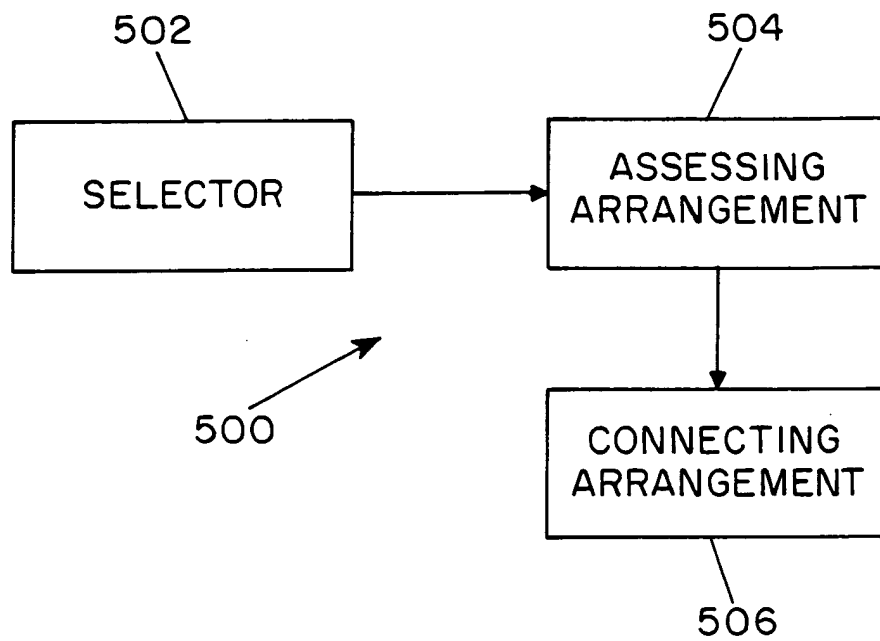
FIG. 3

SoC SPECIFICATION ⟶ 402

CORE LIBRARY ⟶ 406

404 ⟶ DESIGNER SELECTS THE CORES TO BE INSTANTIATED IN THE SoC FROM A CORE LIBRARY

408 ⟶ NETLIST OF UNCONNECTED COMPONENTS

DESIGNER PROVIDES ONE OR MORE LOCAL PROPERTY BINDINGS ⟵ 418

410 ⟶ RUN THE CIE TO INTERCONNECT PINS AUTOMATICALLY

ARE ALL PINS CONNECTED? 412

NO ⟶ LIST OF UNCONNECTED PINS ⟶ 416

YES

COMPLETE TOP-LEVEL NETLIST FOR SoC WITH ALL COMPONENTS FULLY INTERCONNECTED ⟶ 414

400

FIG. 4

502

504

SELECTOR

ASSESSING
ARRANGEMENT

500

CONNECTING
ARRANGEMENT

506

FIG. 5